Challenges and Opportunities for InP HBT Mixed Signal Circuit Technology

John C. Zolper
DARPA/MTO
3701 North Fairfax Drive, Arlington, VA 22213
PH: 703-696-7039, FAX: 703-696-2206
jzolper@darpa.mil

Abstract:

Mixed signal circuits based on InP HBTs are being challenged for meeting DoD high bandwidth and dynamic range requirements by aggressively scaled SiGe bipolar technology. This paper presents the challenges that conventional mesa InP HBT technology must overcome (primarily scaling and integration complexity) to maintain its competitive advantage over the silicon alternative. Approaches to overcoming these challenges are identified.

INTRODUCTION

The fundamental material properties of InP, and related alloys, are exceptionally well suited to high speed, high linearity Heterojunction Bipolar Transistors (HBTs) for high bandwidth, high precision mixed signal circuits. This has been recognized for over 20 years and validated through the performance of both single transistors and state-of-the-art mixed signal circuits. For example, single DHBTs have achieved a combined f_t/f_{max} of 300/300 GHz with BV_{ceo} > 4V and DHBTs have produced 21 dB unilateral power gain at 100 GHz.[1,2] In addition, InP DHBTs have operated in a ring oscillator with 2 ps gate delay and demonstrated a static latch toggling at 100 GHz.[3,4] These transistor and circuit benchmarks are superior to the performance of any other bipolar transistor technology.

HBTs FOR MIXED SIGNAL CIRCUITS

Although InP HBTs have achieved impressive transistor performance, the real metric of interest is circuit performance. Figure 1 shows a plot of small signal unity current gain (f_t) versus reported static flip-flop (SFF) maximum toggle speed with data shown for SiGe HBTs and InP HBTs. Also plotted are lines for constant ratios of flip-flop speed to f_t. Prior to 2002, InP HBTs achieved higher f_t than SiGe but only marginally higher static flip-flop speed (i.e. InP HBT SFF's achieved a lower percentage of f_t than did SiGe). Over the past year, reported InP SFF speed has moved closer to f_t while SiGe HBT SFF speed has remained close to $0.75*f_t$ with the demonstration of a 81 GHz SFF using SiGe HBTs with 140 GHz f_t.[5] The reason for InP HBT SFF's not achieving speeds proportional to their higher

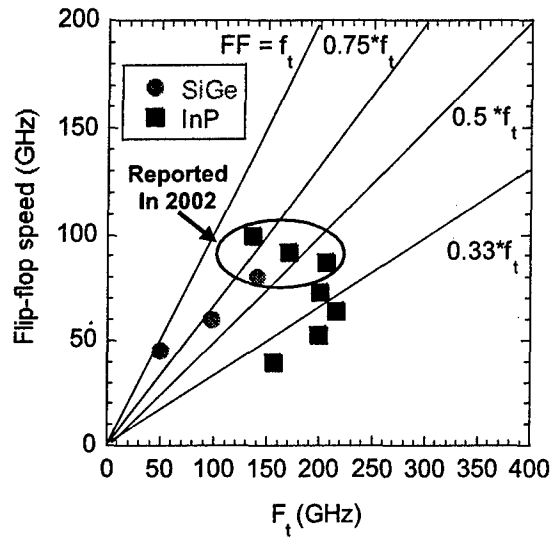

Figure 1: Maximum static flip-flop toggle speed versus f_t for SiGe and InP HBTs. The lines are fixed ratios of flip-flop speed to f_t.*

* Data is only shown for published results where both f_t and static flip-flop speed were reported.

f_t can be found if we consider, in addition to the small signal metrics of f_t and f_{max}, a mixed signal figure of metric (MSFOM) for a transistor technology as being[6]:

$$MSFOM = \frac{J_C BV_{CEO}}{C_{CB} \Delta V_{LOGIC}}$$

where J_c is the current density, BV_{CEO} is the collector-emitter breakdown voltage, C_{CB} is the base-collector capacitance, and ΔV_{logic} is the peak-to-peak logic swing. The MSFOM assumes the transistor technology already has sufficiently high f_t from vertical layer scaling such that the carrier transit delay times do not limit performance. The MSFOM addresses the need to minimize parasitic device capacitance (C_{CB}) and be able to drive high current density (i. e. to rapidly charge device and interconnect capacitances) to achieve high circuit performance. In addition, for high dynamic range mixed signal circuits, a (relatively) large breakdown voltage is advantageous to maintain signal swing and enhance linearity.

To achieve high f_t, f_{max}, J_c, BV_{CEO}, and low C_{CB}, the HBT design must: 1) achieve low base and collector transit times ($\tau_{b,c}$) for high f_t, 2) balance the reduction in collector transit time with the reduction in breakdown voltage (BV_{CEO}) and an increase in C_{CB}, 3) minimize the base access resistance (R_B), 4) minimize the extrinsic base-collector capacitance (C_{CB}), and 5) minimize the emitter contact resistance (R_E) for high J_c.

A mesa HBT with reduced parasitic C_{CB} is represented in Figure 2. The distinguishing features are the use of a highly doped InGaAs base (5-10x10^{19} cm^{-3}), a minimum base contact region and uncut of the collector to minimize C_{CB}, and the use of an InP collector for high breakdown (compared to an InGaAs collectors) with good saturated electron velocity. This approach has been successful for optimization of *discrete* HBTs with emitter feature lengths down to ~0.35 μm with the demonstration of f_t up to 377 GHz and f_{max} over 300 GHz.[1,2,7]

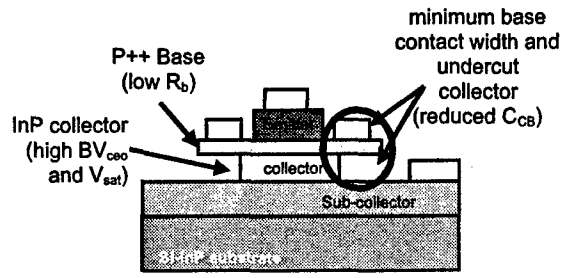

Figure 2: Schematic of InP mesa DBHT.

SiGe CHALLENGE

InP HBT technology can no longer rely solely on epitaxial layer vertical scaling and optimization to give performance superior to alternative technologies. In fact, InP HBT performance is being challenged by aggressively scaled Si CMOS and SiGe bipolar transistor technology. Specifically, SiGe HBTs, currently produced with an emitter length of 0.18 μm and below, have demonstrated a combined f_t/f_{max} of 270/260 GHz and a peak f_t of 350 GHz.[8] The high f_t was achieved with a current density of 20 $mA/\mu m^2$, but with a BV_{CEO} of only 1.4 V. The SiGe HBT performance is enabled by processing technology that reduces the extrinsic base-to-collector capacitance as well as the extrinsic base and emitter access resistance. The Si-based processing employs selective oxidation, local implantation doping, and highly doped regrown polycrystalline silicon to minimize the extrinsic parasitics. In order for InP mixed signal circuits (and also analog and digital circuits) to maintain its differentiating advantage for high end performance, InP technology must also employ aggressive device scaling to produce a high-performance, manufacturable, and highly-integrated circuit technology that extends the speed*power advantage over competing SiGe technology.

SUPER-SCALED InP HBT

A schematic of a representative, super-scaled InP DHBT is shown in Figure 3 with the key technology challenges identified. The structure in Figure 3 incorporates many of the scaling approaches employed by SiGe HBTs. The emitter resistance is minimized by employing a regrown emitter with an expanded contact area to a low bandgap, highly doped InAs layer. The base resistance is minimized by using regrown extrinsic base layers, potentially with a p++ GaSb contacting layer, along with a highly doped intrinsic base. Either a Be or a C doped InGaAs base are options for the intrinsic base as well as C-doped GaAsSb. C_{CB} is minimized by either patterned growth of the base and emitter, selective area doping of the collector by ion implantation, or some combination of these techniques. To maintain a high breakdown voltage and minimize thermal resistance, an InP collector is employed. The DHBT must employ bandgap engineering at the B/C junction to minimize current blocking to allow high current density operation. This can be accomplished either by using base-collector grading or with a type II base-collector band line-up with a GaAsSb-base.

HIGH DYNAMIC RANGE CIRCUITS

The requirements for DoD mixed signal circuits (ADCs and DACs) include high center frequency, bandwidth, and dynamic range. This is driven by the desire to have direct signal generation and sampling into the mm-wave frequency range and the necessity of operating over a large range of signal levels. Fundamental limits to mixed signal circuit dynamic range include: thermal noise, aperture jitter, additive circuit noise, harmonic distortion, element matching, and operating voltage. InP DHBTs have many attractive features, especially once they are aggressively scaled, for producing high frequency and high dynamic range circuits.

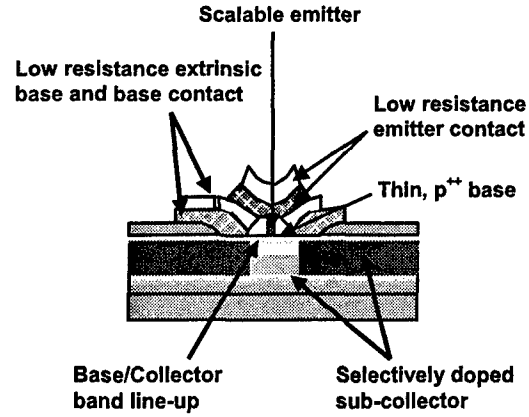

Figure 3: Schematic of a scalable, high performance, InP HBT for mixed signal circuits

BACK END PROCESSING

The realization of a super-scaled InP DHBT will significantly advance mixed signal circuit performance, however, circuit speed is also limited by interconnect parasitics. SiGe circuits have a significant advantage in the back end interconnect technology that has been established for complex CMOS circuits. The fine pitch and multiple metallization levels available in Si foundries allow the circuit designer to closely pack the logic gates and minimize interconnect loading.

InP HBT technology must also incorporate more aggressive interconnect topologies to take full advantage of the transistor performance. Looking back to Figure 1, one of the reasons that SiGe-based flip-flops get speeds closer to f_t is the interconnect technology. Typical InP HBT foundries employ 2 to 3 levels of global interconnects on a course (several μm) pitch for the first level. A minimum of 4 interconnect levels is desirable with micron or below pitch and vertical stacking of vias.

TFAST PROGRAM GOALS

The development of super-scaled InP DHBTs with advanced interconnects to enable complex mixed signal circuit is the goal of the Defense Advanced Research Projects Agency (DARPA) TFAST (Technology for Frequency Agile Digitally Synthesized Transmitters) program. The first phase of the program is a technology development effort with the goals shown in Table I.

Table I: TFAST Program Metrics.

metric	Pre-program	Phase I	Program goal
Emitter width (μm)[(b)]	~1.0	0.25	0.15
f_t/f_{max} (GHz)[(b)]	200/200 (typical)	350/400	500/500
J (kA/cm^2) (at fixed V_{CE})[(b)]	≤200	500	1000
Flip flop speed (GHz) (at fixed power)	75	150	200
Super-scaled integrated transistor count	0	1000	20,000

(b) with $BV_{CEO} \geq 4$ V

The TFAST program is pushing InP HBT technologists to rethink their processing approach and develop radically new techniques to fully exploit InP materials. The processing approaches employ regrown extrinsic regions, dielectric sidewall spacers to control lateral spacings, selective area implantation, and aggressive vertical scaling. The program started in October 2002 with the demonstration of the Phase I metrics planned for early calendar year 2004.

CONCLUSION

InP HBT prominence for high performance mixed signal circuits is being challenged by aggressively scaled SiGe bipolar technology. The TFAST program is striving to produce a leap ahead by developing super-scaled InP HBTs for complex mixed signal circuits that will create a revolutionary capability for future DoD systems.

References:

[1] M. W. Dvorak, C. R. Bolognesi, O. J. Pitts, and S. P. Watkin, IEEE Elec. Dev Letts. 22, 361 (2001).

[2] M. J. W. Rodwell, M. Urteaga, T. Mathew, D. Scott, D. Mensa, Q. Lee, J. Guthrie, Y. Betser, S. C. Martin, R. P. Smith, S. Jaganathan, S. Krishnan, S. I. Long, R. Pullela, B. Agarwal, U. Bhattacharya, L. Samoska, and M. Dahlstrom, IEEE Trans. Electron Dev., 48, 2606 (2001)

[3] N. K. Srivastava, G. Raghavan, R. Thiagarajah, M.G. Case, E. Arnold, C.W. Pobanz, S. O. Nielsen, J. C. Yen, R. A. Johnson, GaAs IC Digest 2002, 171 (2002).

[4] M. Mokhtari, C. Fields, R.D. Rajavel, GaAs IC Digest 2002, 291 (2002).

[5] K. Washio, E. Ohue, R. Hayami, A. Kodama, H. Shimamoto, M. Miura, K. Oda, I. Suzumura, T. Tominari, T. Hashimoto, IEDM-02, p. 767 (2002).

[6] Modified from FOM published by M. J. W. Rodwell et. al; ibid ref 2

[7] W. Hafez, J. W. Lai, and M. Feng, IEEE EDL (accepted for publication).

[8] J. -S. Rieh, B. Jagannathan, H. Chen, K. T. Schonenberg, D. Angell, A. Chinthakindi, J. Florkey, F. Golan, D. Greenberg, S. J. Jeng, M. Khater, F. Pagette, C. Schnabel, P. Smith, A. Stricker, K. Vaed, R. Volant, D. Ahlgren, G. Freeman, K. Stein, and S. Subbanna, IEDM-02, p. 771 (2002).